REQUIREMENTS SPECIFICATION DOCUMENT

SEPHY
Grant No. 640243

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[1] Dissemination level: **PU** = Public; **PP** = Restricted to other programme participants (including the Commission Services); **RE** = Restricted to a group specified by the consortium (including the Commission Services); **CO** = Confidential, only for members of the consortium (including the Commission Services).
[2] Nature of deliverable: **R** = Report; **P** = Prototype; **D** = Demonstrator; **O** = Other

Abstract

The requirements for integrated circuits that have to operate in space are very different from those that are used in terrestrial applications. In particular, the radiation is much more intense and causes several types of effects on the devices that compromise their reliability. Therefore, special "rad-hard" design and manufacturing techniques are needed for devices that will operate in space.

Therefore, in order to implement Ethernet in space systems, rad-hard Ethernet components have to be designed. This deliverable provides the guidelines to design and manufacture rad-hard Ethernet PHYs (Physical layer transceivers). In particular a 10/100Mbps PHY is targeted as the first short term objective. The SEPHY deliverable D2.1 specifies the requirements for the achievement of the project goals, i.e. the implementation of a rad-hard Ethernet transceiver component that can be used in space missions.

Requirements have been analyzed and consolidated in the following categories:

- *Communication and standard compliance*
- *Interfaces*
- *Power and power consumption*
- *Clocks*
- *Environmental (radiation, temperature)*
- *Reliability and fault-tolerance*
- *Configuration*
- *Quality in Manufacturing*

This gathered data will be used as basis for the elaboration of a feasibility and risk assessment document, the PHY architectural design as well as for the creation of validation and verification plans at block, transceiver and network level.

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Document Change Record

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Draft 1	15.07.2015		All	Creation
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Draft 3	21.07.2015		Summary, Acronyms, Methodology	Text added
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Issue 1	31.07.2015		Deliverable D2.1 submitted	Closed deliverable
Draft 5	01.07.2016		Abstract	Text added
Draft 5	01.07.2016		Section 2. Network and application level requirements	Added text to clarify why functional and non-functional requirements encompass
Draft 5	01.07.2016		Section 2. Network and application level requirements	Added text to clarify which clauses of the 802.3 standard will be considered.
Draft 6	15.07.2016		Subsection 2.1 Non-Functional requirements	Edited requirements #5, #6, #15 and #16 to be more precise
Draft 6	16.07.2016		Subsection 2.1 Non-Functional requirements	Added requirement #45, #46 and #47.
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Draft 7	19.07.2016		Subsection 2.2 Functional requirements	Added requirement #44
Issue 2	20.07.2016		D2.1 submitted	Included feedback from review meeting

Disclosure Statement

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1 Introduction

1.1 Objectives

The goal of this Network and Application level Requirements document is to provide detailed definitions of the set of requirements needed for the design and implementation of a 10/100 Ethernet physical layer transceiver.

1.2 Use of the D2.1 outcomes

The requirements are an important basis for other deliveries and work packages of the SEPHY project. They have been specified by the project partners based on their domain of expertise and on those activities to accomplish throughout the course of this project.

Work package WP2 will encompass the conditions to be satisfied for the development of the Ethernet PHY. These play an important role in WP3, for the system design and verification, as well as during the PHY design, fabrication and testing in WP4, WP5 and WP6.

The dependencies between the different work packages are illustrated Figure 1.

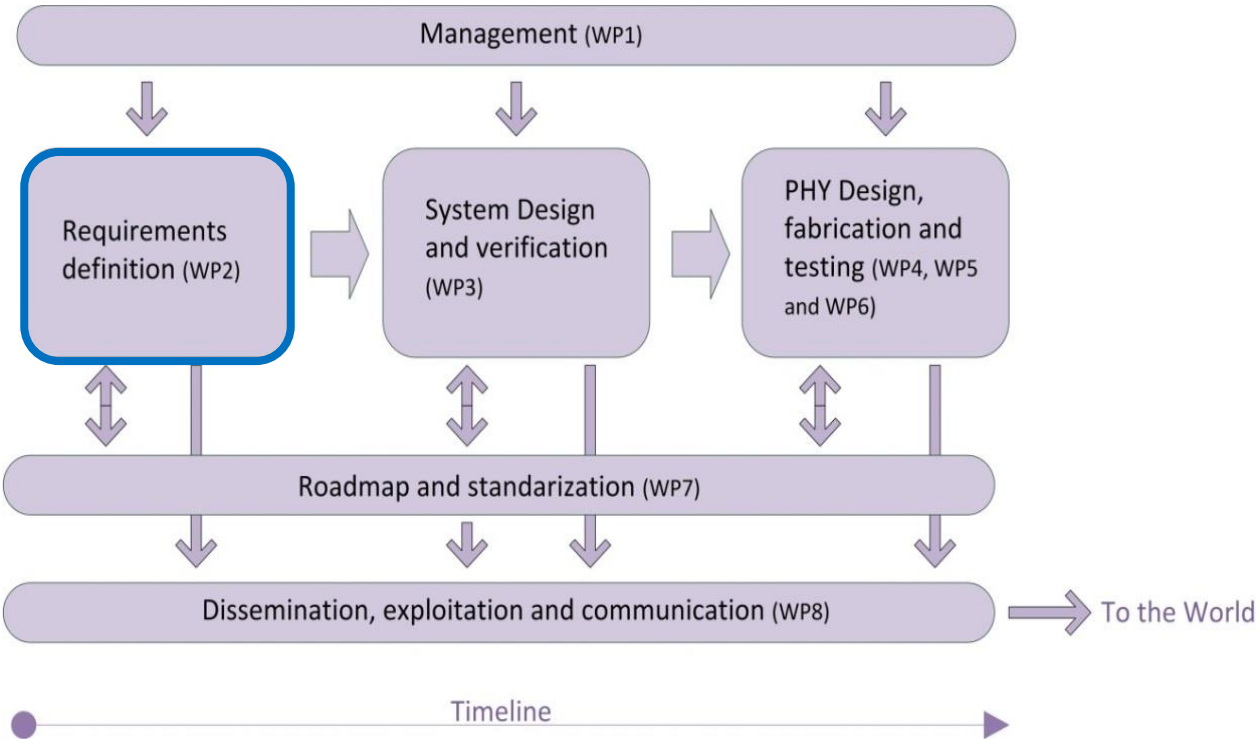

Figure 1. Interactions among all Work Packages

1.3 Methodology used for the requirements definition phase

The goal of this document is to provide a complete set of requirements for the development of the SEPHY transceiver. To this end, each partner has been requested to identify functional and non-functional requirements according to their area of expertise.

Phase 1: Bottom-up requirements collection

The requirements were collected in a bottom-up fashion based on the consortium expertise that covers:

- Analogue and digital design expertise
- Space system architecture expertise
- Manufacturing and process expertise
- Ethernet and standards expertise
- Space market expertise (launchers and satellites)

An input sheet has been provided to be filled with each partner's data as an initial input which was left free in order to come up with bottom-up requirements from each of the expertise areas.

Phase 2: Technical discussion and harmonization

Following the requirement collection phase the technical discussion phase started in order to iterate and align the requirements to each other and to discuss technical feasibility based on mutual understanding of capabilities and technical challenges and work out potential conflicting requirements. A single excel sheet collecting all requirements was created, distributed among the partners and used for discussion. This occurred in an iterative way in three iterations, where each partner had time to make changes to or comment on their own requirements and/or of those of the partners.

Phase 3: Consolidation phase

The consolidation phase aimed to eliminate repeated requirements, assure similar wording, set priorities. A compact version of the outcome of the consolidation phase listing the functional and non-functional requirements can be found in this document. An extended version is available in the Appendix section.

The link between the consolidated requirements and the initial requirements of the partners has been kept to enable backtracking in case of unclear issues.

2 Network and Application level requirements

The network level requirements encompass all functional and non-functional properties that shall be respected regarding the low level functionality of the physical layer. This reflects the requirements as posed by the IEEE 802.3 Ethernet specification, as well as various requirements with respect to operating environment, power consumption, management interface, packaging, and further specific requirements for space Ethernet.

The requirements at application level will provide an overview of those functionalities that the SEPHY chip needs to implement. TASE will, for instance, take the lead based on their experience at equipment, subsystem and system level. TTT will contribute to this task with the TTEthernet level perspective. ATMEL will participate in this task by sharing its extensive customer experience with all partners and will also be able to get specific information from key potential customers and end-users.

The requirements are split in two categories:

1. Non-functional: Composed of five subcategories – Power & Power Consumption, Environmental, Interfaces, Manufacturing, and Reliability and Fault-tolerance– with a total of twenty five requirements, from which twenty three were identified to have high priority and the rest low. Here, Power & Power Consumption as well as the Environmental subcategories turned out to collect most of the non-functional needs. See Figure 1 for a graphical representation.

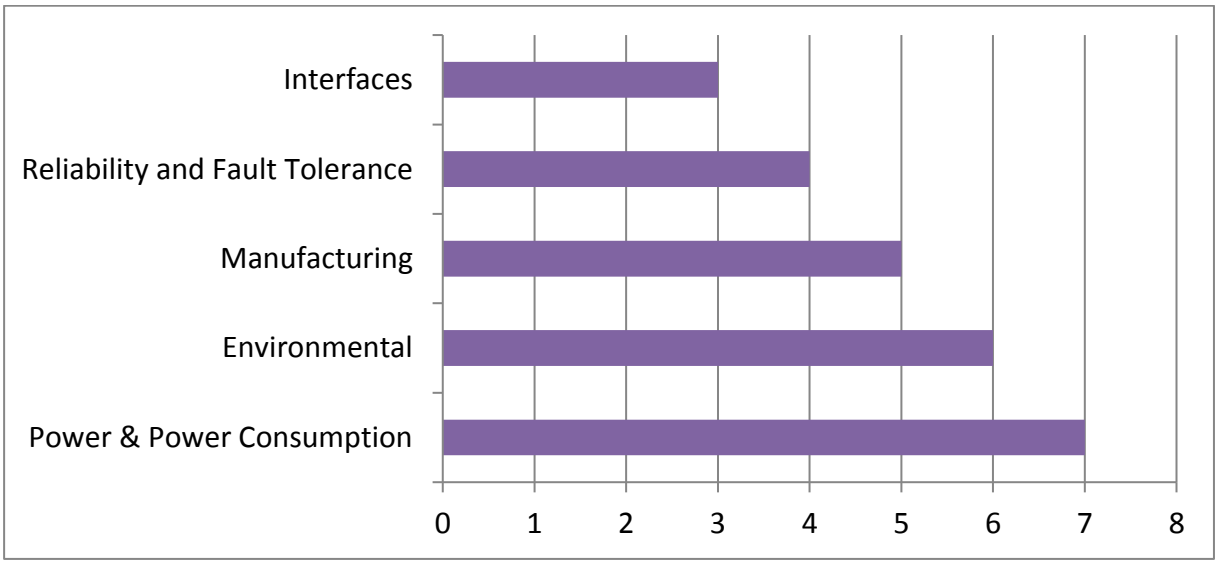

Figure 2. Number of non-functional requirements sorted according to category

2. Functional: Composed of six subcategories – Communication and Standard Compliance, Reliability and Fault-tolerance, Clocks, Interfaces, Configuration, and Manufacturing – with a total of twenty two requirements, where sixteen were identified to be of high priority, one with medium and four with low priority. The subcategories Communication and Standard Compliance collected most of the functional needs together with Reliability and Fault-tolerance. See Figure 3 for a graphical representation.

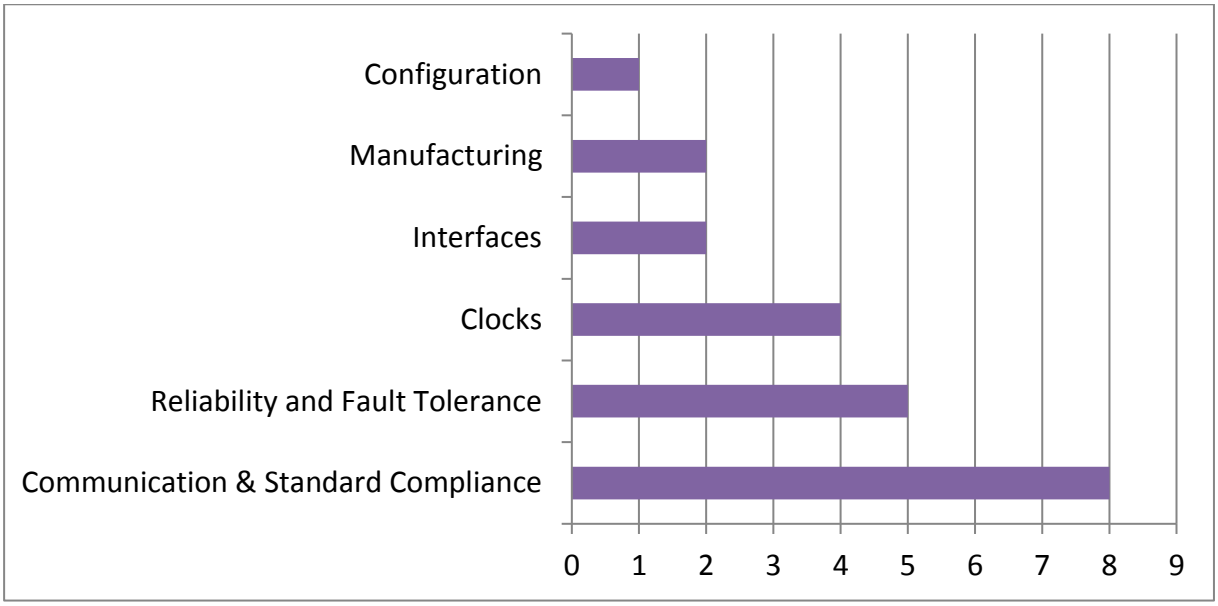

Figure 3. Number of functional requirements sorted according to category

Note that both functional and non-functional requirements comprise manufacturing, reliability & fault tolerance and interfaces sub-categories. The difference here is that non-functional requirements relate to the specification of criteria that is used to judge the operation of the SEPHY PHY. On the other hand, those requirement categories defining specific behaviour or functions fall into the functional requirements category.

A key functional requirement is to be IEEE 802.3 (loose) standard-compliant. This means that basic requirements guaranteeing interoperability with other PHYs and with different MAC (for ground testing and potentially also in a space system) will be considered. This is captured in requirement 10, but deserves a more detailed explanation: the IEEE 802.3 standard is organized in clauses. Each clause covers an independent aspect of the standard, for example a PHY specification for a given speed and media type, a MAC interface or

specific features like auto-negotiation or energy efficient Ethernet. The clauses relevant to SEPHY are those related to 10/100 Mbps[3], namely:

- Clause 14. Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T. This clause details the 10BASE-T PHY specifications.
- Clause 22. Reconciliation Sublayer (RS) and Media Independent Interface (MII). This clause details the 10/100 MAC interface specifications.
- Clause 24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X. This clause details part of the 10BASE-TX PHY specifications.
- Clause 25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX. This clause details part of the 10BASE-TX PHY specifications.

There are a few requirements that are covered in other clauses of the standard. As those are however in most cases less critical, they have been marked as low priority requirements. These include for instance:

- Parallel Detection: Clause 28. Physical Layer link signalling for Auto-Negotiation on twisted pair Parallel detection function section “28.2.3.1 Parallel Detection”.
- Energy Efficient Ethernet: Clause 78. Energy Efficient Ethernet (EEE).

The certification of SEPHY by an independent certification laboratory such as the Interoperability Laboratory at the University of New Hampshire is outside of the scope of the project. However, the verification process has been designed in a way that their test guidelines are followed so that in the future SEPHY could be certified if needed. The tests to be carried out for ensuring a basic level of compliance with the standard are described in detail in the deliverables D3.2 Verification Procedure at block level and D3.3 Verification Procedure at transceiver level.

In regard to those requirements addressing the total dose radiation tolerance (#1, #2, #3, #4 and #17), the following remark should be stated: the exact dose rates and the possible dose-rate effects that will be used for testing SEPHY (in the core MOS devices and/or in the bipolar devices used in the bandgap reference) will be specifically included in the test plan. These values will be described in detail in the D6.8 Radiation Plan and Report 1.

A compact version of the non-functional and functional requirements for both network and application level requirements is now introduced. Note the latter information before going through the tables:

- The word “Type” offers information regarding what type of requirement is evaluated.

[3] For 100Mbps over twisted pair there are several PHY alternatives in the IEEE 802.3 standard like 100BASE-T4 or 100BASE-T1. For SEPHY only the 100BASE-TX option is relevant as it is the one implemented.

- “Requirements ID”: each requirement is associated to a specific ID. This is helpful in case more specific information is searched in the extended excel sheet (see Appendix).

- “Description”: provides an explanation of the requirement itself and what the devices or functions “shall” do.
  The word "shall" identifies mandatory provisions of this document. It is reserved exclusively for requirements and must not be used for any other meaning. A requirement must contain only one "shall".

- "Priority": This allows to identify the importance level of a requirement. “High” means that this is important to accomplish and “Low” is something that it is important to have, but it does not have major consequences if not achieved.

2.1 Non-Functional Requirements

Type	Req. ID	Description	Priority
Environmental	1	The Total Ionizing Dose (TID) shall be greater than 100krad. SEPHY regards this value, as it is used by most of the space applications.	High
	3	The SEU threshold LET shall be at least 30MeV/mg/cm². It is important that the PHY supports operation under radiation conditions in deep space environment.	High
	4	The SEU Error Rate, considering GEO orbit, shall be lower than 10^-10 errors/bit-day (at <70 MeV/mg/cm²). It is important that the PHY supports operation under radiation conditions in deep space environment.	High
	17	The SEL Threshold LET shall be greater than 70 MeV/mg/cm². This is the maximum value that can be measured in European accelerators. It is necessary that the PHY supports operation under radiation conditions in deep space environment.	High

	2	The Total Ionizing Dose (TID) shall be greater than 300krad. This is the maximum TID value tested so far, and has low priority as it cannot be ensured.	Low
	5	During the test sequence, the chip shall withstand temperatures in the range of -55°C to +125°C. The operating environment in spacecraft fluctuates greatly in temperature and the chip should thus be able to endure this.	High
Manufacturing	6	The PHY shall be designed to be manufactured for space-grade ceramic (ESCC9000 or QML-V) and plastic packaging. The flexibility of packaging will support different customer requests: ceramic for launchers and plastic for development purposes.	High
	13	The package shall be of Quad Flat type (QFP) and shall have a maximum of 64 pins. A standard space package will be considered for design purposes.	High
	34	There shall be no floating grounds.	High
	45	The chip shall be at least MSL1, hermetic for ceramic package and MSL3, non-hermetic for plastic package.	High
	46	A traceability of the chips in the supply chain shall be possible.	High
Power and power consumption	12	The analogue and digital power domains shall be separated.	High
	14	The digital domain shall have its own external 1.8V supply. Fast switching digital supply voltage should be provided externally, as some electronic components are difficult to integrate on-chip.	High
	11	The analogue domain shall have its own external 3.3V supply.	High

	15	ESD tolerance shall be 2 kV HBM (Class 2 / MIL-STD-883H), 250V in CDM and higher than 100V in MM.	High
	26	Special care shall be put during power supplies sequencing during start-up, to avoid excessive inrush-current.	High
	29	The power dissipation shall be lower than 0.5W.	High
	43	The PHY shall meet a power consumption target of <0.5W. This should enable its use in a wide range of applications that are power limited.	High
Reliability and Fault-tolerance	16	Chip lifetime in space environment shall be 20 years in GEO for the ceramic version and 10 years for the plastic version. The expected lifetime of the device has a big impact on the implementation of the chip.	High
	23	The design shall accommodate manufacturing testability. It is important to provide adequate test interfaces and/or specifications that allow for efficient and automatic testing.	High
	25	Fault-tolerant techniques that are used during the VHDL development phase shall be defined. It is important to regard the possible fault effects on the higher level of the digital design hierarchy, such as in counters, registers, reset and clock generation circuits.	High
	47	The reliability of the chip shall be 1000 FIT. This will ensure that the number of failures is at most in the order of 1000 devices for 1 million hours.	High
Interfaces	27	Digital interfaces shall be implemented with LVCMOS/LVTTL compatibility.	High
	31	An Enable function shall be externally provided through a pin.	High

	28	The transmitter and receiver interface shall be compatible with cold spare. It is meaningful to have high-impedance output and input pins for redundancy (when needed).	Low

2.2 Functional Requirements

Type	Req. ID	Description	Priority
Interfaces	7	Access to the PHY for data transfer shall be provided to the MAC by means of an RMII and MII interface. A standard interface for data communication to the MAC layer should be guaranteed.	High
	8	Access to the PHY for management and diagnostics shall be provided to the MAC by means of an MDIO interface. A standard interface for management and diagnostics to the MAC layer should be provided.	High
Clocks	9	The minimum MDIO clock rate shall be at least 2.5MHz. Again, for validation purposes, a standard interface for management and diagnostics to the MAC layer should be provided.	High
	18	A clock (CLKIN) shall be externally provided through a pin. A clean external clock is the best reference source for clocking the device.	High
	19	CLKIN shall be 25MHz. It should be compatible with other devices.	High
	20	CLKIN clock jitter shall be 250 ps. This is important for	Medium

		the PLL design.	
Communication and standard compliance	10	The PHY shall be loose IEEE 802.3 standard-compliant with the clauses that are relevant to 10/100 over twisted pair. In more detail, the following clauses should be implemented: - Clause 14. Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T - Clause 22. Reconciliation Sublayer (RS) and Media Independent Interface (MII) - Clause 24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X. - Clause 25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX.	High
	21	The PHY shall operate always in full duplex mode. There is no shared media allowed for UTP.	High
	35	In terms of latency, the PHY shall support a TTL between 250 and 500ms.	High
	42	The PHY shall support a cable length of up to 100m. Since the power consumption is nearly the same for 50m & 100m, the selected cable length is 100m.	High
	37	The PHY shall support Parallel Detection (not full Auto-negotiation).	Low
	38	The PHY shall support frame lengths of up to 8000 bits.	Low
	40	The PHY shall support Energy Efficiency Ethernet (802.3az) by manual configuration (no Auto-negotiation)	Low
	41	The PHY shall also support 100-BASE-FX for optical media to cover a wider market.	Low
Configuration	22	All configuration registers shall be refreshed by	High

		scrubbing. It is necessary to avoid the accumulation of errors in those configuration registers that are not continuously updated.	
Manufacturing	24	Respect the 150nm design manuals rules/guidelines. In this way it is possible to guarantee the product manufacturing capabilities at space level quality.	High
	44	The chip shall be RoHS compliance. Dangerous substances commonly used in electronic and electronic equipment should be avoided.	High
Reliability and Fault-tolerance	30	The PHY shall support Local Loopback mode for self-testing.	High
	32	The PHY shall provide status indicators during operation: Transmission, receptions & link activity pins. This should facilitate the interpretation of any hardware test and diagnostic procedures.	High
	33	The PHY shall integrate internal registers to monitor faults during radiation testing.	High
	36	The PHY shall support link integrity checking for cable diagnostics, as it is part of the standard.	High
	39	The PHY shall support loopback modes for testing and when debugging installed devices. This will allow to perform several types of diagnostics.	High

3 Summary

This document provides a list of Network and Application level Requirements that will be used throughout the course of the SEPHY project for the design, implementation and validation of the 10/100 Ethernet physical layer transceiver.

All these requirements were carefully selected by the partners to ensure that they are fully in line with the trend towards Ethernet based technologies for space applications.

4 Acronyms

CSMA/CD	Carrier Sense Multiple Access with Collision Detection
ESCC 9000	European Space Components Coordination – Generic Specification No. 9000
ESD	Electro Static Discharge
FIT	Failures In Time
IEEE	Institute of Electrical and Electronics Engineers
LET	Linear Energy Transfer
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor Transistor Logic
MAC	Media Access Control
MDIO	Management Data Input/Output
MII	Media-Independent Interface
MSL	Moisture Sensitivity Level
PDK	Process Design Kit
PHY	PHYsical layer
PLL	Phase Locked Loop
QFP	Quad Flat Package
QML	Qualified Manufacturers List
RH	Relative Humidity
RMII	Reduced Media-Independent Interface
SEL	Single Event Latch-up
SEPHY	Space Ethernet PHYsical layer
SEU	Single Event Upsets
TID	Total Ionizing Dose
TTL	Time to leave
UTP	Unshielded Twisted Pair
VHDL	Very High Speed Integrated Circuits
WP	Work Package

5 Appendix

Requirement ID: <Req. ID>	Category <Functional / non-Functional>	Sub Category <Radiation, Temperature, Packaging, etc>	Description: <Req. Description>	Verification Method <Description how to verify>	Rationale: <The rationale behind this req.>	Priority <High, Medium, Low>
1	Non-Functional	Radiation	Total Ionizing Doze (TID) shall be greater than 100krad.	Radiation testing (T6.3.2, T6.3.4)	The PHY shall support operation under radiation conditions in deep space environment.	1 - High
2	Non-Functional	Radiation	Total Ionizing Doze (TID) shall be greater than 300krad.	Radiation testing (T6.3.2, T6.3.4)	The PHY shall support operation under radiation conditions in deep space environment.	3 - Low
3	Non-Functional	Radiation	The SEU threshold LET shall be at least 30MeV/mg/cm²	Radiation testing (T6.3.3, T6.3.5)	The PHY shall support operation under radiation conditions in deep space environment.	1 - High
4	Non-Functional	Radiation	The SEU Error Rate shall be lower than 10^-10 errors/bit-day (at <70 MeV/mg/cm²)	Radiation testing (T6.3.3, T6.3.5)	The PHY shall support operation under radiation conditions in deep space environment.	1 - High

5	Non-Functional	Temperature	The chip shall withstand temperatures in the range of -55°C to +125°C.	Temperature testing	Operating environment in spacecraft fluctuates greatly in temperature.	1 - High
6	Non-Functional	Packaging	The PHY shall be available in space-grade ceramic and plastic packaging	Inspection	Flexibility of packaging will support different customer requests.	1 - High
7	Functional	Interfaces	Access to the PHY for data transfer shall be provided to the MAC by means of an RMII and MII interface	Functional testing (T6.2.2, T6.2.3)	Provide standard interface for data communication to the MAC layer.	1 - High
8	Functional	Interfaces	Access to the PHY for management/diagnostics shall be provided to the MAC by means of an MDIO interface.	Functional testing (T6.2.2, T6.2.3)	Provide standard interface for management/diagnostics to the MAC layer.	1 - High
9	Functional	Speed	The minimum MDIO clock rate shall be at least 2.5MHz.	Functional testing (T6.2.2, T6.2.3)	Provide standard interface for management/diagnostics to the MAC layer.	1 - High

10	Functional	Standard compliance	The PHY shall be loose IEEE 802.3 standard-compliant with the clauses that are relevant to 10/100 over twisted pair. In more detail, the following clauses should be implemented: - Clause 14. Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T - Clause 22. Reconciliation Sublayer (RS) and Media Independent Interface (MII) - Clause 24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X. - Clause 25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX.			1 - High

11	Non-Functional	Power	The analogue domain shall have its own external 3.3V supply	Inspection	see ARQ-003	1 - High
12	Non-Functional	Power	Separated analogue and digital power domains	Inspection	Avoid interferences between analogue and digital domains	1 - High
13	Non-Functional	Packaging	The package shall be of QFP type and shall have a maximum of 64 pins	Inspection	A standard space package is recommended	1 - High
14	Non-Functional	Power	The digital domain shall have its own external 1.8V supply	Inspection	Fast switching digital supply voltage it is better to be externally provided since big capacitors are difficult to integrate on-chip	1 - High
15	Non-Functional	Power	ESD tolerance shall be 2 kV HBM (Class 2 / MIL-STD-883H) and 250V in CDM.	Inspection		1 - High
16	Non-Functional	Reliability	Chip lifetime in space environment shall be 20 years in GEO for the ceramic version and 10 years for the plastic version. The expected lifetime of the device has a big impact on the implementation of the chip.	Analysis	The expected lifetime of the device has a big impact on chip implementation	1 - High

17	Non-Functional	Radiation	The SEL Threshold LET shall be greater than 70 MeV/mg/cm²	Radiation testing (T6.3.3, T6.3.5)	The PHY shall support operation under radiation conditions in deep space environment.	1 - High
18	Functional	Clocks	A clock (CLKIN) shall be externally provided through a pin	Inspection	A clean external clock is the best reference source for clocking the device.	1 - High
19	Functional	Clocks	CLKIN shall be 25MHz	Inspection	Compatibility with other devices	1 - High
20	Functional	Clocks	CLKIN clock jitter shall be 250 ps	Inspection	Required for PLL design	2 - Medium
21	Functional	Communication	The PHY shall operate always in full duplex mode	Verification and Functional testing	No shared media is allowed for UTP.	1 - High
22	Functional	Configuration	All configuration registers shall be refreshed by scrubbing.	Verification and Functional testing	Avoid the accumulation of errros in configuration registers that are not continuously updated	1 - High

23	Non-Functional	Quality	The design shall accommodate manufacturing testability	Manufacturing testability review	Provide adequate test interface/specification to allow efficient automatic test (probe/test)	1 - High
24	Functional	Quality	Respect 150nm Design Manuals rules/guidelines	Run geometric checker, connectivity checker and DRV checker.	Guarantee the product manufacturing capability at space level quality	1 - High
25	Non-Functional	Fault-tolerance	Fault-tolerant techniques that are used during the VHDL development phase shall be defined	Basic functional testing with fault-injection	As the flip-flop cells, from Atmel RH standard cell library are already TMR based it is important to take care about fault effects on the higher level of the digital design hierarchy - counters, registers, reset and clock generation circuits, etc.	
26	Non-Functional	Power supply	Special care shall be put during power suplies secuencing durning start-up, to avoid excesive inrush-current.	Design		1 - High

27	Non-Functional	Interfaces	Digital interfaces shall be implemented with LVCMOS/LVTTL compatibility.	Functional testing (T6.1)		1 - High
28	Non-Functional	Interfaces	The TX/RX interface shall be compatible with cold spare	Functional testing (T6.1)	High-impedance output/input pins for redundancy in case needed	3 - Low
29	Non-Functional	Power dissipation	The power dissipation shall be lower than 0.5W	Functional testing (T6.1)		1 - High
30	Functional	Self-test	The PHY shall support Local Loopback mode.	Functional testing (T6.1)	PHY testing (T6.1 & T6.3) & BIST	1 - High
31	Non-Functional	Interfaces	An Enable function shall be externally provided through a pin	Functional testing (T6.1)	Power control	1 - High
32	Functional	Operation	The PHY shall provide status indicators: TX, RX & Link activity pins	Functional testing (T6.1)	Hardware diagnostic & test	1 - High

33	Functional	Fault-tolerance monitoring	The PHY shall integrate internal registers to monitor faults during radiation testing	Radiation testing (T6.3)	A method to monitor detection and correction errors will be required to validate fault-tolerance techniques.	1 - High
34	Non-Functional	Packaging	No floating grounds	Design	Package groung plane.	1 - High
35	Functional	Latency	Time to link (delay from power up to packet transmission)	Verification and Functional testing	The PHY shall support a TTL between 250 and 500ms.	1 - High
36	Functional	Cable Diagnostics	Support Cable diagnostics	Verification and Functional testing	The PHY shall support link integrity checking, as it is part of the standard.	1 - High
37	Functional	Auto-Neg	Parallel Detection	Verification and Functional testing	The PHY shall support Parallel Detection (not full autoneg).	3 - Low
38	Functional	Packet length	Jumbo frames	Verification and Functional testing	The PHY shall support frame lenghts of up to 8000 bits.	3 - Low
39	Functional	Diagnostics	Loopback modes: RMII,PCS,PMD,AFE	Verification and Functional testing	They PHY shall support loopback modes for testing and debugging installed devices.	1 - High

40	Functional	Energy Efficiency	Energy Efficiency Ethernet (802.3az)	Verification and Functional testing	The PHY shall support Energy Efficiency Ethernet by manual configuration (no Autoneg).	3 - Low
41	Functional	Fiber	Support 100-BASE-FX	Verification and Functional testing	The PHY shall also support 100-BASE-FX for optical media to cover a wider market.	3 - Low
42	Functional	Cable length	Define the cable lenght supported by the PHY	Verification and Functional testing	The PHY shall support a Cable length of up to 100m.	1 - High
43	Non-Functional	Power Consumption	Target power consumption in 10/100	Functional testing	The PHY shall meet a power consumption target of <0.5W to enable its use in a wide range of applications that are power limited.	1 - High
44	Functional	Quality	The chip shall be RoHS compliant	Design	Any RoHS compliant component should be tested for the presence of Lead (Pb), Cadmium (Cd), Mercury (Hg), Hexavalent chromium (Hex-Cr), Polybrominated biphenyls (PBB), and other dangerous substances commonly used	1 - High

					in electronic and electronic equipment.	
45	Non-Functional	Packaging	The chip shall be at least MSL1, hermetic for ceramic package and MSL3, non-hermetic for plastic package.	Design	While MSL1 will ensure unlimited floor life (30 °C/85%RH) MSL3 will guarantee 168 hours of exposure time to ambient room conditions (30 °C/60%RH).	1 - High
46	Non-Functional	Manufacturing	A traceability of the chips in the supply chain shall be possible.	Inspection	Tighter inventory control, complying with specific regulations and responding to recalls.	1 – High

47	Non-functional	Quality	The reliability of the chip shall be 1000 FIT.	Functional testing	Ensure that the number of failures is at most in the order of 1000 devices for 1 million hours.	1 – High