A Methodology to Verify Digital IP's Within Mixed-Signal Systems

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***Abstract*—This paper describes a methodology to improve the quality of verification and an approach to dimension the arithmetic of register transfer level (RTL) model of the digital part of the mixed-signal system. This includes the refinement of the high level model of the system and generation of a MATLAB fixed-point model and test-bench for MATLAB-HDL co-simulation. Additionally an approach for the dimensioning of an adaptive equalizer in frequency domain is discussed. The proposed methodology and results of analysis are applied to verify 10BASE-T / 100BASE-TX Ethernet PHY IP.**

Keywords—10BASE-T/100BASE-TX Ethernet PHY, fixed-point model, co-simulation, quantization effects, system verification methodology, test-bench.

I. INTRODUCTION

The advance in the integration possibilities of the analog and digital circuits has increased the complexity of mixed-signal systems. Functional verification of such complex systems is challenging, and there is a need for an optimized system verification methodology. In traditional verification approach, digital intellectual properties (IP's) are verified using pure digital simulations and analog IP's are checked separately at the block-level using analog simulation environment. At the chip level, only a connectivity check is performed to verify the integration of the black box (analog block which is assumed to be pre-verified). Today's complex mixed-signal systems require full-chip verification that covers all possible analog and digital interactions. Formal black-box verification approach that provides no visibility into signals is no longer applicable [1]. Verification using analog mixed signal (AMS) simulation provides high accuracy of the obtained results by enabling the simulation of the entire design as a system, but with a limitation of longer simulation time [2]. As the analog and digital IP blocks can be represented using schematics, SPICE netlists, analog behavioral models, or purely digital models, it is essential to use a hierarchical verification approach [1]. A verification method that supports different levels of abstraction, and uses the integration of high-level MATLAB models for analog components with the digital components, can provide low runtime in comparison to AMS simulation [3]. This verification method can be further enhanced to obtain high performance and accuracy.

This paper describes such an optimization technique by implementing the fixed-point model of the digital components and, co-simulate and verify the digital components within a mixed-signal environment. In addition, the quantization effects in an adaptive equalizer are analytically investigated and a method to dimension the design arithmetic is described.

Adaptive filters within a mixed-signal system contributes to a significant part of the circuit-area and power consumption. Design implementation can be made efficient by selecting the appropriate resolution for these filters. This can be performed by utilizing the fundamentals of digital signal processing (DSP) techniques and fixed-point filter design methods [4]. This paper describes one such approach, where the optimal coefficient width of an adaptive equalizer can be theoretically deduced through frequency-domain simulations [5]. Although simulation analysis might not cover all possible scenarios of system behavior, this method can provide a basis for simple and faster approximation of optimal resolution.

With the possibility of faster development of fixed-point model and co-simulation of digital blocks with the run-time of few minutes, the proposed verification methodology highly improves the mixed-signal verification quality.

This paper is divided into 5 sections. The fundamentals of proposed verification methodology are explained in section II. In section III, is presented the implementation of methodology in an example Ethernet PHY 100BASE-TX receiver. Results and important observations are discussed in section IV. In the last section, the paper is concluded by a discussion on the future use of proposed verification methodology.

II. SYSTEMATIC APPROACH

A systematic approach of the verification flow followed in this work is illustrated in the Figure 1. The important step is to create fixed-point models of the digital blocks to be verified, using the corresponding floating-point model.

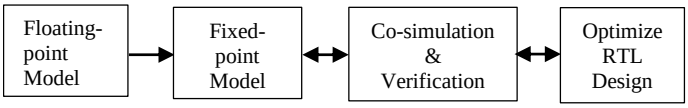

Fig. 1. Proposed system verification methodology to verify digital IP's in a mixed-signal environment

Then a test-bench is created to co-simulate the fixed-point model with the RTL design of the corresponding digital block. The design is further optimized by analyzing the quantization effect, dimensioning and re-verification.

A. System Dimensioning

Quantization errors introduced in the system due to finite precision arithmetic can be analyzed to select optimal resolution of the design. Digital blocks using an adaptive

system have a large number of arithmetic operations, therefore increasing the possible quantization error. Hence the design optimization of an adaptive equalizer is considered in this work.

In digital filters with fixed-coefficients, quantization errors may originate from analog to digital conversion (ADC), coefficients quantization or from round-off during multiplications, considering that overflow is prevented through scaling. In addition, more quantization noise will be generated in an adaptive system due to multiplication operations involved in updating the filter coefficients [6]. A cable-channel model is implemented and optimal resolution for the design is proposed based on the frequency response and quantization error calculations.

In general, the proposed method can be applied to verify an entire communication system with a transmitter and a receiver. The implementation of the methodology is discussed in detail in the following section.

III. Implementation

The Space Ethernet PHYsical (SEPHY) layer transceiver, 100BASE-TX receiver design was used as a reference to evaluate the proposed verification methodology.

The SEPHY project targets the implementation of the 10BASE-T and 100BASE-TX standards. This will provide 10 Mb/s and 100 Mb/s connectivity in space systems.

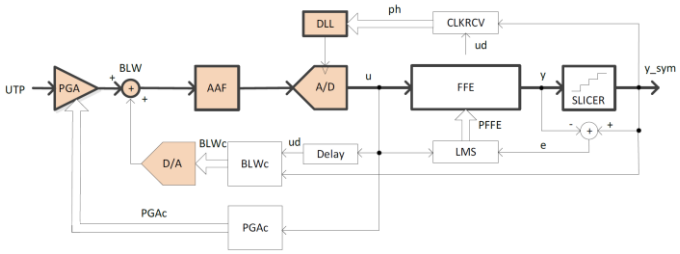

Fig. 2. SEPHY 100BASE-TX receiver architecture with analog and digital blocks

Figure 2 shows the 100BASE-TX receiver architecture with the analog (colored blocks) and the digital blocks. This work focuses on the verification of digital blocks which are introduced in the next sub sections.

A. Baseline Wander Controller (BLWc)

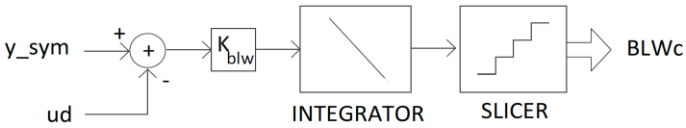

Fig. 3. BLWc Architecture

BLWc detects and corrects the slow drifts in the average received signal and the direct current (DC) offset. The architecture of BLWc is illustrated in Figure 3. Subtracting the delayed ADC output from the equalized and quantized FFE output *y_sym* gives the error signal. The error signal is then multiplied with the K_{BLW} factor of 1/512, integrated and quantized to 7-bit signal same as that of the digital to analog converter (D/A) resolution.

B. Clock Recovery (CLKRCV)

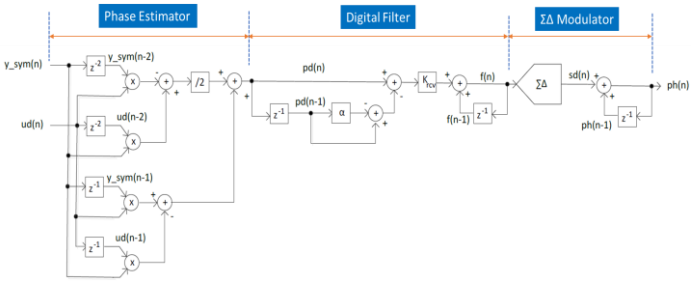

Fig. 4. ClkRcv Architecture

Timing information from the received signal is recovered at the clock recovery block to process the data synchronously. The architecture of the block, shown in Figure 4, consists of a phase estimator implemented using Mueller-Muller algorithm, a digital filter and a first order ∑Δ-modulator.

C. Programmable Gain Amplifier Controller (PGAc)

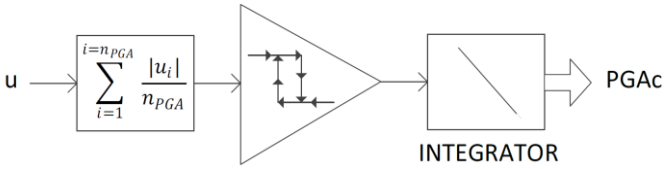

Fig. 5. PGAc Architecture

PGAc controls the gain level of the PGA to avoid saturation and to achieve rated precision of ADC. This block performs the average of absolute value of the input (ADC output) which is then compared with the digital hysteresis comparator threshold, and the hysteresis default value. The output from the comparator is integrated to obtain the output, which has the same resolution as that of the PGA gain levels. The integrator value will be modified by +1/0/-1 depending on the comparator output.

D. Feed Forward Equalizer (FFE)

An equalizer compensates the distortions and inter symbol interference (ISI) caused by the bandwidth limited channel, and improves the receiver performance. An FFE consists of a digital FIR filter with 14 taps.

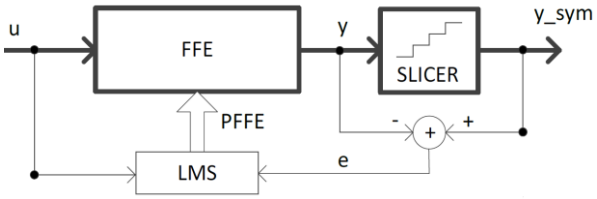

Fig. 6. FFE Architecture

The FFE coefficients (P_{FFE}) are computed adaptively using Least Mean Square (LMS) algorithm on every clock cycle using the following equations:

$$P_{FFE}(n) = P_{FFE}(n\text{-}1) + \mu \cdot e(n) \cdot u(n) \quad (1)$$

$$e(n) = y(n) - y\_sym(n) \quad (2)$$

where, μ is a constant, *y_sym* is the output of the slicer and *y* is the output of the FFE filter.

E. *Fixed-point implementation and Co-simulation*

Fixed-point model was implemented by converting all the floating-point arithmetic to fixed-point in the code algorithm. This implementation can be explained using the following steps:

1. Code implementation using fixed-point data types and constructors. MATLAB constructors such as *fi* and *fimath* constructors were used to create fixed-point objects and perform fixed-point arithmetic.
2. Writing a test file and validation by comparing with the floating-point algorithm results.
3. Code acceleration and report generation. The command *fiaccel* was used to build MATLAB executable (MEX) file for the floating-point algorithm and fixed-point data type report was generated. This report was used to compare the proposed word length (WL) with that of the data type used in the fixed-point model code algorithm and correct the model [7].

Better performance can be obtained by utilizing the code generation and instrumented MEX. Selection of precision while converting to fixed-point model and compatibility of the algorithm for code generation could be challenging in this implementation [7].

Once the fixed-point model was implemented, RTL design was verified by MATLAB-HDL co-simulation. An algorithm to communicate with the HDL simulator was written as a test-bench function in MATLAB. After creation of a test-bench function, below mentioned procedure was followed:

1. Socket communication on port 4449 was setup using *hdldaemon* command.

2. RTL design of the corresponding digital block was loaded in HDL simulator and initialized using *matlabtb* command. This work uses Cadence SimVision™ tool as HDL simulator and VHDL for programming.

3. Once the link is established, HDL simulator functions as the client as shown in the Figure 7. When the server receives the request, the corresponding MATLAB function is executed.

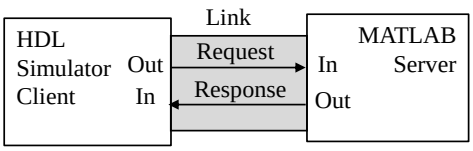

Fig. 7. Linking with MATLAB server and HDL simulator client [8]

4. The output port signal values from the HDL simulator can be obtained from *oport* structure in the MATLAB server. HDL client communicates with the server every 5 ns until the session is active.. Verification is done by plotting and comparing the results with fixed-point and floating-point model results [8].

F. *Analytical approach to select optimal resolution*

As a next step, to analyze the quantization effects in FFE, frequency responses of simple coax-cable channel model and Ethernet PHY cable channel model with infinite precision are compared.

Relationship between channel-equalizer combined impulse response and error can be deduced from Figure 8.

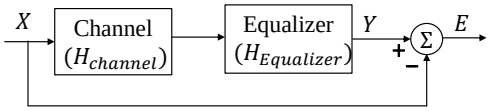

Fig. 8. Channel-Equalizer Model

The error between the transmitted and the received sequence in frequency domain can be obtained by,

$$E(z) = Y(z) - X(z) \qquad (3)$$

$$= X(z) \cdot (H(z) - 1)$$

Where, $H(z) = H_{Channel}(z) \cdot H_{Equalizer}(z)$

If the equalizer is close to ideal, then

$$H_{Equalizer}(z) \approx 1 / (H_{Channel}(z))$$

$H(z) \approx 1$, *hence* $E(z) \approx 0$.

But due to coefficient quantization,

$$H^*(z) = H_{Channel}(z) \cdot (H_{Equalizer}(z) + H_{quant}(z))$$

Therefore,

$$E(z) = X(z) \cdot (H^*(z) - 1) \qquad (4)$$

In practice, the equalizer cannot be ideal thus the error cannot be zero. A threshold value for the error is fixed, as per the specification.

The above mentioned model is implemented in MATLAB using simple coax-cable channel and LMS adaptive filter. Filter coefficients are quantized using fixed-point arithmetic in MATLAB and the error between the transmitted and the equalized sequences are simulated. Change in the frequency response due to quantization effect is observed. Considering FFE block of an Ethernet PHY receiver, same method is applied for the analysis. Power spectral density (PSD) estimate of quantization error was observed and a resolution was selected such that this quantization error remains below certain threshold.

IV. Results and Discussion

The simulation results of implemented fixed-point models, floating-point models are compared with the corresponding RTL design simulations. Figures 9, 10 and 11 show the model simulations for BLWc, CLKRCV and PGAc digital blocks.

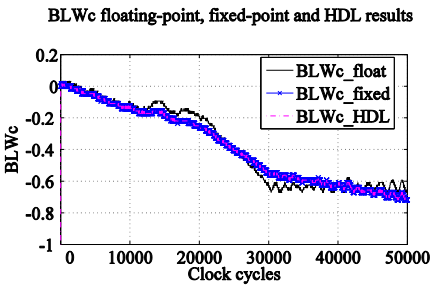

Fig. 9. Linking with MATLAB server and HDL simulator client

In these digital block simulations, RTL design is verified by obtaining no error between the fixed-point model and the design simulations. Fixed-point and floating-point model simulations show a difference due to the selected fixed precision in the fixed-point model. This difference is observed to be $2^{-\text{fractional bits}}$ in every fixed-point arithmetic conversion from floating-point arithmetic.

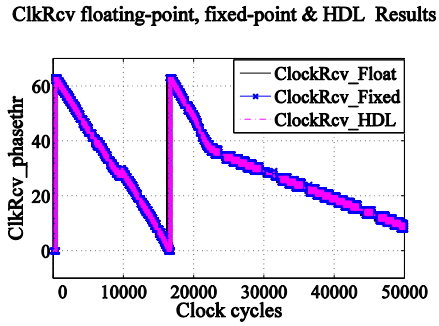

Fig. 10. Simulation results of floating-point, fixed-point and HDL implementations of ClkRcv

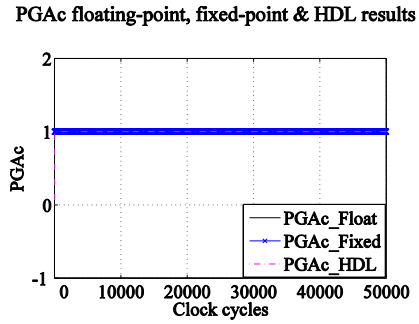

Fig. 11. Simulation results of floating-point, fixed-point and HDL implementations of PGAc

As a part of system dimensioning, the combined frequency response of coax-cable channel-equalizer model and the Ethernet PHY-FFE model in SEPHY system, shows the inverse relation to channel frequency response. With the decrease in the resolution in terms of word length (WL), the frequency response shows a deviation from the desired result. The error term calculated using equation 4, increases with the increasing quantization effects due to decrease in WL.

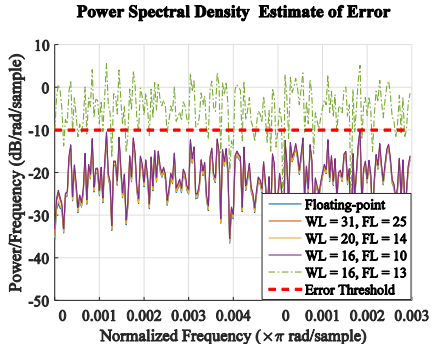

Fig. 12. Increase in PSD of error due to quantization effects in FFE

The PSD estimate of the error in Figure 12 shows that a WL of 16-bits and fraction length (FL) of 13-bits, is not suitable for the SEPHY design. The quantization error increases due to insufficient precision for integer part. A resolution is selected such that the error remains below chosen threshold value. From the simulation results, resolution of 16-bit with 6-bit integer part and 10 bit fractional part can be selected for SEPHY system such that the power/frequency remains below -10 dB

V. Conclusion

A method of verification presented in this paper, significantly reduces the effort needed in the verification of digital IP's within complex mixed-signal system and ensures additional correctness compared to the existing multi-layer verification. Theoretical simulations of quantization effects and dimensioning of an adaptive equalizer can provide an estimation to achieve cost-effective, efficient design.

This method can be further enhanced, by improving simulation time and extending quantization error analysis to other blocks of the design.

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References

[1] S. Balasubrahmanian, P. Hardee, "Solutions for Mixed-Signal SoC Verification Using Real Number Models", Cadence Design Systems, 2013, pp. 1-4.

[2] M. Nizic, "Mixed-signal Design Trends and Challenges; Overview of Mixed-signal design Methodology," in Mixed-signal Methodology Guide, B. Bailey, Ed., San Jose, CA, Cadence Design Systems, Inc., 2012, pp. 2–24.

[3] A. Breitenreiter, J. López , P. Reviriego, Eine Methode zur Verifikation von Mixed-signal-ASIC(March, 2017), at 29. Workshop Testmethoden und Zuverlässigkeit von Schaltungen und Systemen, Lübeck.

[4] P. Reviriego, C. Murray, "DSP Dimensioning of 1000Base-T Gigabit Ethernet PHY ASIC", Massana Technologies, Madrid, Spain, January, 2002.

[5] R. B. Abreu, L. Cordeiro, et.al., "Verifying Fixed-Point Digital Filters using SMT Based Bounded Model Checking", at SBRT, Fortaleza, MA, CE, 2013.

[6] M. Freire, "Eficient Implementation for Systems with Adaptive Filters," M. Sc. dissertation, Dept. Elect. & Comp. Eng., Instituto Superior Técnico, Lisboa, Portugal, 1993.

[7] MathWorks, "Fixed-Point Designer™ User's Guide," Natick, MA,The MathWorks, Inc., March 2017, pp. (1-2) –(4-2), (8-1) – (8-86).

[8] MathWorks, "HDL Verifier™ User's Guide," Natick, MA, The MathWorks, Inc., Mar. 2017, pp. (1-2) – (2-41).

[9] P. Reviriego, J. López et. al.,"The Space Ethernet PHYsical Layer Tranceiver (SEPHY) Project: A Step Towards Reliable Ethernet in Space," IEEE A&E Systems Magazine, pp. 24–28, Jan. 2017, 10.1109/MAES.2017.1600