TWO-FOLD RADIATION HARDENING APPROACH:

The SEPHY transceiver will undergo:

- * Radiation hardening by design: special circuit design techniques that can be applied at the system, architectural or layout level, e.g.: EDAC, TMR.
- * Process hardening: modifications during fabrication processes to reduce the impact of radiation on integrated circuits, e.g.: use of specific insulator materials or the modification of doping profiles.

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FUNCTIONAL AND ENVIRONMENTAL (RADIATION) TESTING:

- * The SEPHY results will be tested in a radiation environment measuring all the electrical parameters. In particular, Total Ionizing Dose (TID), Single Event Upset (SEU) and Single Event Latch-up (SEL) tests will be performed.
- * Estimate the overall performance of the space qualified communication system built around the SEPHY device.
- * Determine the amount of communication errors induced in the system by the radiation effects.
- * The PHY behavior will be tested with regards to standard Ethernet and Time-Triggered Ethernet functionality.
- * All tests guarantee that the SEPHY device achieves a high maturity level such that it will be ready for qualification at the end of the project

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SPACE-QUALIFIED MANUFACTURING AND PACKAGING:

- * The chip will achieve manufacturing which is fully compliant with already existing quality standards and reliability requirements.
- * The chip will be available in space-grade ceramic and plastic packaging to support different customer requests. The package will be Quad Flat type (QFP), with a maximum of 64 pins.
- 5 SUPPORT EUROPEAN PACKAGING OF NAKED COMPLEX MULTIPAD DIES AND MIXED ASIC TESTING CAPABILITIES:
- * The Ethernet PHY will be a mixed-signal device packaged and tested within Europe.

SEPHY SPACE ETHERNET PHYSICAL LAYER TRANSCEIVER

Project partners:















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Project website: www.sephy.eu
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Disclaimer: The opinions expressed and arguments employed herein do not necessarily reflect the official views of the REA.

The SEPHY consortium brings together a team of recognized partners to achieve the objectives planed within the project. It is composed of 4 industrial companies, 1 research center and 1 leading university, with roots in four European countries.

These partners combine their experience in the areas of analogue and digital design, manufacturing. mixed-signal methodology, fault-tolerant techniques for space electronics and Time-Triggered Ethernet to deliver a first-class device for space applications.