D7.2 REPORT ON TECHNICAL FEASIBILITY OF SPACE GRADE 1GBPS ETHERNET TRANSCEIVERS

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Abstract

An analysis of the requirements of the different alternatives to implement a 1Gbps Ethernet transceiver for Space was presented in the deliverable "D7.1 Report on Requirements for space grade 1Gbps Ethernet transceivers". Based on this analysis, two options were short listed as initial candidates: 1000BASE-T and 2.5GBASE-T. In this deliverable a more detailed feasibility analysis is done for both options considering the implementation in the technology used in SEPHY (Microchip 150nm SOI) and in the nodes that could be used for the next European technology qualified for space.

[1] Dissemination level: **PU** = Public; **PP** = Restricted to other programme participants (including the Commission Services); **RE** = Restricted to a group specified by the consortium (including the Commission Services); **CO** = Confidential, only for members of the consortium (including the Commission Services).
[2] Nature of deliverable: **R** = Report; **P** = Prototype; **D** = Demonstrator; **O** = Other

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Issue 3	20/04/2018	3	Minor changes	Revision for 3rd year review
Issue 4	08/05/2018	4	Section 4	Updated information regarding the timeline for 28nm and 22nm technology nodes in space

Disclosure Statement

Table of Contents

List of Tables

List of Acronyms

ACRONYM	MEANING
AAF	Anti Aliasing Filter
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
ENOB	Effective Number of Bits
LDPC	Low Density Parity Check
SEPHY	Space Ethernet PHY
PAM	Pulse Amplitude Modulation
PGA	Programmable Gain Amplifier
TC2	Test Chip 2
UTP	Unshielded Twisted Pair

Table 1 – List of acronyms.

Executive Summary

This deliverable presents a feasibility analysis of two alternatives to implement space grade 1Gbps Ethernet transceivers. The two options studied: 1000BASE-T and 2.5GBASE-T were selected based on a requirement study presented in D7.1 Report on Requirements for space grade 1Gbps Ethernet transceivers. The feasibility is studied for four technologies: Microchip 150nm, ST 65nm and 28nm and GF 22nm SOI technologies. The first, is the one used in SEPHY and therefore more accurate estimates can be provided. The others are candidates for the next European technology qualified for space. In this case, the estimates are less accurate and based on some expected scaling for analog and digital blocks.

1 Introduction

As mentioned in the abstract, two options have been shortlisted for the implementation of a 1Gbps Space grade Ethernet transceiver. These options are:

- 1000BASE-T (IEEE 802.3ab, 1999).
- 2.5/5GBASE-T (IEEE P802.3bz).

The target implementation technologies are 150nm SOI (the one used in SEPHY) and 65nm 28nm and 22nm SOI from ST and GF. As the clock frequencies used in those options are at most 200 Mhz, both technologies should be able to meet the speed requirements. Therefore, the feasibility of both options depends mainly on the following parameters:

- Die size.
- Power Consumption.

The rest of this document presents estimates for both parameters for each technology. Then, the requirements in terms of die size and power consumption for space PHYs are discussed and compared with the estimates to determine the feasibility.

2 Methodology

To provide a total estimate for the PHY, it is divided in blocks. Then the die size and power are estimated for each block and added to obtain the final estimate. Only the major blocks are modelled as those will determine the die size and power consumption. The blocks for each of the options are described in the following.

2.1 Option 1: 1000BASE-T

In this case, all the blocks run at 125 Mhz. The main blocks are:

- Four ADCs with an ENOB of 5-7 bits.
- Four DACs and line drivers.
- Four Adaptive Equalizers with ~10 taps and precision of > 8bits.
- Four Echo cancellers and twelve near end crosstalk cancellers with a 5 value input and >8 bit coefficients. In total approximately ~1000 taps.
- A Viterbi decoder.

2.2 Option 2: 2.5GBASE-T

In this case, all the blocks run at 200 Mhz. The main blocks are:

- Four ADCs with an ENOB of 6-7 bits.
- Four DACs and line drivers.
- Four Adaptive Equalizers with ~14 taps and precision of > 8bits.
- Four Echo cancellers and twelve near end crosstalk cancellers with a 5 value input and >8 bit coefficients. In total approximately ~1400 taps.

- An LDPC decoder.

3 Estimates for the Different Technology Nodes

As discussed before, the TC2 estimates are the starting point that are then scaled to account for differences in frequency, resolution and technology node. They are presented in the next subsection along with the scaling that will be used for each node.

3.1 Block Estimates for TC2 and Scaling Factors

The initial estimates for each block are taken from SEPHY first test chip (TC2) and are summarized in Table 2. For the digital only the FFE is taken into account as most of the area and power is used there and it is the most similar block to the other adaptive filters (Echo and crosstalk cancellers) that are needed for Gigabit.

Block	Power	Area
Analog TX	74.0mW	0.38 mm^2
Analog RX	112.4mW	0.70 mm^2
FFE	297.1mW	2.33 mm^2

Table 2 – Estimates for the TC2 main blocks

The scaling factors used for each technology versus the 150nm node of TC2 are shown in Table 3. It can be seen that the area scaling will benefit more the digital blocks as it is commonly assumed. For power the scaling is assumed to be the same in both cases.

Node	Power both	Area analog	Area digital
65nm	0.43	0.43	0.188
28nm	0.18	0.18	0.035
22nm	0.15	0.15	0.022

Table 3 – Scaling factors for power and area

3.2 Option 1: 1000BASE-T

The initial estimates for each block are taken from SEPHY first test chip (TC2) in 100BASE-TX mode that has the same frequency as 1000BASE-T. The modifications made are:

- The analog rx is scaled by two to model the additional resolution needed in the ADC as for Gigabit we will need at least one additional bit.

- The FFE is scaled by two to account for the other adaptive filters (one echo canceller and three crosstalk cancellers per pair) that are simpler in resolution but have more taps.
- Four instances of each block are added as in 1000BASE-T we use the four pairs.

This gives the total estimates shown in Table 4. The results suggest that this option is feasible for 28 or 22 nm. Implementing it with a larger node will result in an excessive power consumption.

Mode	Power	Area
150nm	3568mW	25.8 mm^2
65nm	1544mW	6.6 mm^2
28nm	665mW	1.9 mm^2
22nm	521mW	1.5 mm^2

Table 4 – Estimates for the 1000BASE-T option

To better understand the estimates, it is interesting to discuss a number of points:

- The TC2 design can be optimized (see [RD 2]). In particular, it seems that savings of 30-40% on TC2 FFE can be achieved.
- The estimates do not account for the common analog blocks (mainly the PLL). However, those are expected to have a smaller contribution on Gigabit.
- Some digital blocks like the MAC interface and other small blocks have not been included in the estimates. Again those are expected to have a smaller contribution on Gigabit.
- The Viterbi decoder has not been included in the estimates. This digital block can have a relevant contribution especially for larger nodes (due to timing constraints on the critical paths).

3.3 Option 2: 2.5GBASE-T

As in the first option, the initial estimates for each block are taken from SEPHY first test chip (TC2) in 100BASE-TX mode. However, in 2.5GBASE-T the clock frequency is 200Mhz instead of 125Mhz. This has two important implications. The first one is that the adaptive filters will need 60% more coefficients as the impulse responses will have more samples. The second one is that power consumption will also increase with clock frequency. To account for these and other differences with TC2, the following modifications have been made:

- The analog rx is scaled by two to model both the additional resolution needed in the ADC and the speed.
- The FFE is scaled by three to account for the other adaptive filters (one echo canceller and three crosstalk cancellers per pair) that are simpler in resolution but can have more taps and also for the increase in the number of coefficients due to the 200Mhz sampling.
- Four instances of each block are added as in 2.5GBASE-T we use the four pairs.
- The power consumption estimates are increased by 60% to account for the increase in the clock frequency.

The estimates are shown in Table 5. It can be observed that again a small node should be used to get close to a power consumption of 1Watt. We however should also bear in mind that we are getting 2.5x the speed of 1000BASE-T

Mode	Power	Area
150nm	7610mW	35.1 mm^2
65nm	3293mW	8.3 mm^2
28nm	1418mW	2.3 mm^2
22nm	1106mW	1.7 mm^2

Table 5 – Estimates for the 2.5GBASE-T option

As with the 1000BASE-T options, it is interesting to discuss a number of points:

- The TC2 design can be optimized (see [RD 2]). In particular, it seems that savings of 30-40% on TC2 FFE can be achieved.
- The estimates do not account for the common analog blocks (mainly the PLL). However, those are expected to have a smaller contribution on Gigabit.
- Some digital blocks like the MAC interface and other small blocks have not been included in the estimates. Again those are expected to have a smaller contribution on Gigabit.
- The LDPC decoder has not been included in the estimates. This digital block can have a relevant contribution especially for larger nodes (due to critical paths in timing as for the Viterbi decoder).

4 Requirements and discussion

Although there is no hard requirement on die size and power consumption for an Ethernet PHY to be used in space, there are some practical considerations that will limit the use of transceivers that exceed certain values. Those include:

- Integration with other components (such as MAC or switch) on the same die.
- Encapsulation.
- Impact on overall power budget for the system.

Form a system level perspective, a 1 Watt consumption for the PHY seems a reasonable goal according to TASE and TTT inputs. For example, existing SpaceWire PHYs have a power consumption of approximately half a watt [RD1]. The main factor that limits the power consumption is that on a system there can be many transceivers. For example, if we have a system with 40 NICs with 2 ports (redundant) each and 4 switches we end up with 2x40 + 4x20 = 160 Ethernet transceivers. Assuming we have ~10% running at 1Gbit/s speed, we will have a power consumption of 140x0.4 + 20x1=76W only for the transceivers. Since this is point to point, there are 2 transceivers needed for a single link and this results in a high overall power consumption. Therefore the 1G/s SEPHY transceiver should aim for a consumption of 1 Watt.

Based on the requirements and the estimated power consumption, it seems that the next generation of SEPHY should target an advanced technology node. In particular 28nm or 22nm should be used to achieve a power consumption that does not exceed 1 Watt. It seems that the 22nm SOI technology from Global Foundries is gaining interest for space applications. Therefore, if a rad-hard library is available, it would be the preferred option to implement the second generation of SEPHY. At the time of writing this deliverable, there was no timeline for the availability of new nodes for mixed signal for space from Microchip. The consortium was also not aware of any timeline for such a node by other companies. Therefore, a critical point for the next generation of SEPHY is that a 28nm or smaller node for mixed signal space ASICs is available or at least under development by 2021. The information available was that ST is working on the digital library for space for their 28nm SOI technology. The node may be available for mixed signal around 2021. As for the 22nm node from Global Foundries, there are some proposals to develop a rad-hard digital library but not activity has started yet. Therefore, this node is not expected to be available for space applications before 2022. This information will be revised an updated in D7.3 at the end of the project to try to propose a node for the next generation of SEPHY.

As for the option to implement, if the 22nm node is used, both 1000BASE-T and 2.5GBASE-T would be feasible. Therefore, the choice of which one to implement should be driven by considerations on compatibility with existing ground equipment and other developments of Ethernet for space (switches) and also on the roadmap to a third generation. It seems that 1000BASE-T would have advantages on the first two while 2.5GBASE-T would be better in terms of evolution to 5 and 10 Gb/s. Those points will be addressed in D7.3: Report on Comparison and selection of space grade 1Gbps Ethernet transceivers.

References

[RD 1] UT200SpWPHY01 SpaceWire Physical Layer Transceiver Datasheet, Aeroflex, February 2008.
[RD 2] Report on optimized PHY for power and performance, Deliverable D4.29, SEPHY.